Physical Design Engineer Resume

★★★★★ **2.00** /5 (Submit Your Rating)

SUMMARY:

- Proven experienc e as a CPU Design Engineer in Intel's Server Produc t Development Group. Experienc ed in managing multiple stakeholders and c ustomers like RTL front - end
- Validation, and Circ uit/Physic al teams, to enable suc c essful tapeouts ac ross Intel’s servers and c hipsets on 14nm, 22nm and older proc esses. Experienc ed in EDA tools like Synopsys DC, ICC, ICC2-DP, ICValidator
- Timing, Power grid distribution, Bloc k integration and Physic al Verific ation), along with fixing and validating pre- and post-silic on bugs. Owned sign-off of multiple high speed sec tions for Floorplanning/Layout, Cloc king, Power reduc tion, Noise elimination, Reliability
- Verific ation (IR, ESD, EM, SH), and Physic al Design Verific ation. Expertise with 10nm design environment, flows, tools, optimization methods, and physic al imple mentation of SoC sub-c omponents.
- Mentored junior team members to be suc c essful and produc tive. Suc c essfully worked with numerous internal and external c ustomers to enable on- time projec t c ompletion. Solid understanding of the
- IC design and fabric ation flow, lithography, IC fabric ation and design for manufac turability issues. Familiarity and experienc e with power-on bring up, data c apture, software interfac ing and diagnostic s of digital c amera sensor boards.

PROFESSIONAL EXPERIENCE:

Physical Design Engineer

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Responsibilities:

- Closed 2 c ritic al, large, c omplex 500k+ gate bloc ks in Ivytown server projec t, meeting aggressive sc hedule deadlines
- Resolved Sec tion noise violations ac ross two c omplex Ivytown sec tions from hundreds down to zero
- Reduc ed bloc k Noise simulation runtimes from hours to minutes by flow partitioning/paralleliz

ing

- Improved Min delay and ECO rerouting flows on Jaketown server projec t saving 4 weeks of sc hedule
- Identified shortc omings in the Timing improve ment rec ipes/toolkits that led to fine tuning of solutions for all sec tion owners and saved 2 weeks of sc hedule
- Root-c aused and fixed hundreds of Noise violations due to extrac tion issues with c ross -sec tional repeater routing broken at sec tion boundaries
- Sc ripted c onversion of an Exc el deleted sequential waivers file, automatic ally and on demand, into a c sv file in Unix referenc ed by the Jaketown Flow Manager for all bloc k runs and whic h signific antly helped reduc e/ratify the unwaived/waived deleted sequentials enabling high-c onfidenc e tapeout
- Drove impleme ntation of c ritic al DFX signal routing ac ross numerous sub-sec tions working with Cloc k and DFX team members whic h ensured c ontinuity ac ross various die c hops
- Resolved problems with the DC timing/c onstraints setup to enable signific ant reduc tion in timing paths and early c losure of bloc ks to pull-in the Jaketown tapein sc hedule by 2 weeks
- Pioneered the imple mentation and testing of the Timing Wall Optimization f low in Jaketown whic h showed a marked improveme nt in the timing wall with c loc k buffer insertion in DC - Topo and ICC stages, helping reduc e bloc k c losure times and the tapeout sc hedule
- Pioneered a new Cloc k+DFX net routing methodology for several bloc ks in high speed I/O sec tions

Senior Component Design Engineer / Verification Engineer

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Responsibilities:

- Enabled on- time/high quality tapeouts with ownership of physic al design imple mentation of several partitions, whic h involved tasks ranging from c loc k tree synthesis to DFT and physic al design verific ation
- Impleme nted automated partition DFT DRC statistic s c ollec tion thorough sc ripts that quic kly provide d key indic ators of the health of the design and enabled easy trac king c apabilities in SharePoint
- Automated running of partition level Sc an DFT DRC c hec ks, providing c omprehensive partition status within 2 hours of DC netlist synthesis
- Root-c aused Sc an DRCs by learning Verilog HDL and provided feedbac k to RTL team
- Analyzed untestable faults through TetraMax and improved ATPG fault c overage further by 0.4%
- Impleme nted and tested MBIST (Memory Built -In Test) methodology with RTL team

Component Design Engineer / Verification Engineer

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Responsibilities:

- Captured and proc essed digital c amera sensor images from capture boards and generated c olor image s from raw sensor data using C++ proc essing
- Pioneered a hierarc hic al Sc an insertion methodology using DFTAdvisor
- Supervised a web developer intern in the development of the Division's website designed to bec ome a c enter of c ollaboration
- Divisional Rec ognition s for Operational Exc ellenc e/Produc tivity by Improving RTL-tapeout throughput time from 12 to 6 weeks
- Fabric Chipset Division Rec ognition - Demonstrating the first func tional InfiniBand Fabric at 2001 IDF